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10/774,418

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L6 and ((avoid or avoiding) near10 (etching or etch or etched))	0

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DATE: Sunday, December 12, 2004 [Printable Copy](#) [Create Case](#)

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DB=USPT; PLUR=YES; OP=ADJ

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<u>L8</u>	L6 and ((avoid or avoiding) near10 (etching or etch or etched))	0	<u>L8</u>
<u>L7</u>	L6 and (avoid near3 (etching or etch or etched))	0	<u>L7</u>
<u>L6</u>	L5 and (etching)	20	<u>L6</u>
<u>L5</u>	11 and L4	20	<u>L5</u>
<u>L4</u>	(porous near2 (low adj K))	184	<u>L4</u>
<u>L3</u>	L1 near6 (porous near2 (low adj K))	0	<u>L3</u>
<u>L2</u>	L1 near6 (porous near (low adj K))	0	<u>L2</u>
<u>L1</u>	plasma near5 (copper or cu)	1684	<u>L1</u>

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Search Results - Record(s) 1 through 10 of 20 returned.

☐ 1. Document ID: US 6821884 B2

L6: Entry 1 of 20

File: USPT

Nov 23, 2004

US-PAT-NO: 6821884

DOCUMENT-IDENTIFIER: US 6821884 B2

TITLE: Method of fabricating a semiconductor device

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWC	Draw D
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☐ 2. Document ID: US 6806182 B2

L6: Entry 2 of 20

File: USPT

Oct 19, 2004

US-PAT-NO: 6806182

DOCUMENT-IDENTIFIER: US 6806182 B2

TITLE: Method for eliminating via resistance shift in organic ILD

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWC	Draw D
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☐ 3. Document ID: US 6797630 B1

L6: Entry 3 of 20

File: USPT

Sep 28, 2004

US-PAT-NO: 6797630

DOCUMENT-IDENTIFIER: US 6797630 B1

TITLE: Partial via hard mask open on low-k dual damascene etch with dual hard mask (DHM) approach

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWC	Draw D
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☐ 4. Document ID: US 6794311 B2

L6: Entry 4 of 20

File: USPT

Sep 21, 2004

US-PAT-NO: 6794311

DOCUMENT-IDENTIFIER: US 6794311 B2

TITLE: Method and apparatus for treating low k dielectric layers to reduce diffusion

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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☐ 5. Document ID: US 6784109 B2

L6: Entry 5 of 20

File: USPT

Aug 31, 2004

US-PAT-NO: 6784109

DOCUMENT-IDENTIFIER: US 6784109 B2

TITLE: Method for fabricating semiconductor devices including wiring forming with a porous low-k film and copper

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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☐ 6. Document ID: US 6737747 B2

L6: Entry 6 of 20

File: USPT

May 18, 2004

US-PAT-NO: 6737747

DOCUMENT-IDENTIFIER: US 6737747 B2

TITLE: Advanced BEOL interconnect structures with low-k PE CVD cap layer and method thereof

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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☐ 7. Document ID: US 6716693 B1

L6: Entry 7 of 20

File: USPT

Apr 6, 2004

US-PAT-NO: 6716693

DOCUMENT-IDENTIFIER: US 6716693 B1

TITLE: Method of forming a surface coating layer within an opening within a body by atomic layer deposition

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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☐ 8. Document ID: US 6686273 B2

L6: Entry 8 of 20

File: USPT

Feb 3, 2004

US-PAT-NO: 6686273

DOCUMENT-IDENTIFIER: US 6686273 B2

TITLE: Method of fabricating copper interconnects with very low-k inter-level insulator

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw D
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☐ 9. Document ID: US 6673725 B2

L6: Entry 9 of 20

File: USPT

Jan 6, 2004

US-PAT-NO: 6673725

DOCUMENT-IDENTIFIER: US 6673725 B2

TITLE: Semiconductor device and method of manufacturing the same

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw D
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☐ 10. Document ID: US 6638875 B2

L6: Entry 10 of 20

File: USPT

Oct 28, 2003

US-PAT-NO: 6638875

DOCUMENT-IDENTIFIER: US 6638875 B2

TITLE: Oxygen free plasma stripping process

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw D
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L6: Entry 10 of 20

File: USPT

Oct 28, 2003

DOCUMENT-IDENTIFIER: US 6638875 B2

TITLE: Oxygen free plasma stripping process

Brief Summary Text (6):

Fabrication of integrated circuits using copper interconnects and low k dielectrics present new challenges and problems for the semiconductor manufacturer. In order to make these devices, the manufacturers commonly use a damascene process. The damascene process uses most of the same chipmaking technologies to form the interconnect as the traditional structure but differs in the way the structure is built. Instead of etching a pattern in a metal film and surrounding it with dielectric material, a damascene process etches a pattern into a dielectric film, then fills the pattern with copper. An advantage to damascene processing is that the metal etch is replaced by a simpler dielectric etch as the critical step that defines the width and spacing of the interconnect lines. One of the problems manufacturers must overcome occurs after the pattern is etched into the low k dielectric layer. The photoresist used to define the metal circuit pattern into the low k dielectric layer and any post etch residues including sidewall polymer deposition need to be thoroughly removed or stripped from the underlying layer. The existing stripping processes are not adequate for removing photoresist and post etch residues from low k dielectric surfaces.

Brief Summary Text (9):

One problem with oxygen containing plasmas is that they are generally unsuitable for use with copper and most low k interconnects. The etch selectivity of the oxygen containing plasma with low k dielectric materials is generally poor, especially for those low k dielectrics that are organic. The materials used for the photoresists are similar to those used for the low k dielectric materials. That is, both materials are easily oxidized by an oxygen containing plasma to form volatile by-products. As a result, the low k materials are removed at roughly the same rate as photoresist by an oxygen plasma, making the ash selectivity of photoresist to low k materials close to unity. Even using very dilute oxygen mixtures, which at the same time significantly slows the ashing reaction, has not overcome this problem. The challenge is to remove photoresist and post etch residues subsequent to lithography and etch processes without affecting the pattern etched into the low k dielectric layer. Small deviations in the etched profiles can adversely impact device performance, yield and reliability of the final integrated circuit.

Brief Summary Text (10):

Copper is a readily oxidizable, ductile material and as such, is prone to oxidation with the use of oxygen containing plasmas. The build-up of copper oxide from exposure to oxygen containing plasmas is detrimental to device performance. Higher contact resistance results which impedes the flow of current through the integrated circuit. Consequently, clock speed and electromigration can be affected.

Brief Summary Text (11):

Another problem with the use of the oxygen plasma on low k dielectric layers is that the oxygen plasma has been found to change the dielectric constant during ashing. For example, it has been found that doped oxide low k materials, such as nanoglasses and aerogels, exposed to the oxygen containing plasma result in an increase in the dielectric constant. An increase in dielectric constant undesirably

affects interconnect capacitance and cross talk. It is believed that this is due to the oxidation of the Si--H and Si--OH bonds to form Si--O bonds. Still further, the use of an oxygen plasma with integrated circuits having copper as the interconnect tends to oxidize the exposed copper surface and deleteriously affect device performance.

Brief Summary Text (19):

In a particularly preferred embodiment, the plasma gas comprises a mixture of a forming gas and a carbon tetrafluoride gas. The preferred forming gas comprises a mixture of a hydrogen gas and a nitrogen gas wherein the hydrogen gas ranges in an amount from about 3 percent to about 5 percent by volume of the forming gas. The carbon tetrafluoride gas is less than about 10 percent by volume of the total plasma gas. The substrates to be stripped by the plasma are preferably heated from about 80.degree. C. to about 350.degree. C. to accelerate the reaction time and maximize throughput. For organic low k materials the wafers are preferably heated from about 80.degree. C. to about 180.degree. C. The plasma produces fluorine and hydrogen reactive species that are electrically neutral and charged particles thereof. The charged particles are selectively removed prior to reaching the reaction chamber. The neutral species of the plasma reacts with the photoresist and the post etch residues to produce volatile alkanes. More preferably, the neutral species reacts with the photoresist and the post etch residues to produce methane gas as the principal reaction product. Preferably the etching selectivity of the plasma between the photoresist and/or post etch residues, and a substrate is at least greater than about 10 to 1.

Detailed Description Text (2):

The present invention is directed to a method of using an oxygen free plasma gas composition for removing photoresist and/or post etch residues from semiconductor wafers by means of a non-oxidative chemical reaction. The oxygen free plasma comprises a hydrogen bearing gas and a fluorine bearing gas. The invention is especially suitable for use with those substrates employing copper interconnects and low k dielectric insulating layers. Low k dielectrics are hereinafter defined as those insulating materials suitable for use in the manufacture of integrated circuits or the like having a dielectric constant less than about 3.5. Low k dielectrics can be generally categorized as one of three types: organic, porous or doped oxides. Examples of organic low k dielectric materials suitable for use in the present invention include polyimides, benzocyclobutene, parylenes, and fluorocarbons. Examples of porous low k dielectric materials include nanoporous oxides and organic polymers such as those sold under the tradenames NANOGLASS and AEROGEL. Examples of doped oxide low k dielectric materials include hydrogen silsesquioxanes, nanoporous oxides, organic polymers, and carbon doped silicon dioxides available under the trade name CORAL and hybrid materials available under the trade name HOSP. Other low k dielectric materials will be apparent to one of ordinary skill in the art in view of this disclosure.

Detailed Description Text (6):

The damascene process is shown occurring on an underlying first metal layer generally designated 10 having a completed metal interconnect and dielectric layer. The first step in the fabrication of each copper interconnect level is deposition of a thin layer of silicon nitride 12 as shown in FIG. 1A. The nitride layer acts a barrier against diffusion of copper between metal levels and also serves as an etch stop in a dielectric etch process. In FIG. 1B, deposition of a thick low k dielectric layer 14 immediately follows deposition of the nitride etch stop layer. The low k material may have a thin layer of oxide on an upper surface. The dielectric layer is patterned by conventional photo-lithographic techniques using a photoresist 16 as a masking material to form the vias as shown in FIG. 1C. The photoresist is coated onto the low k dielectric layer, patterned by exposure to activating energy, and subsequently developed to form a relief image. In FIG. 1D, the relief image is then partially etched into the dielectric layer using conventional etching techniques known to those skilled in the art. The photo-

lithographic process is repeated to form a trench layer and subsequently etched as shown in FIGS. 1E and 1F. As shown in FIGS. 1G through 1I, a copper metal deposition process is used to fill the spaces left by the etching and stripping processes to form the second metal layer. Current copper deposition techniques require the deposition of a barrier layer that also acts as a seed layer 17 for subsequent copper deposition as shown in FIG. 1G. After the copper 18 has been deposited the wafer surface is then planarized typically by a chemical and mechanical polishing step. The processes are then repeated and the integrated circuit or the like is formed.

Detailed Description Text (7):

After each etching step, any photoresist and/or post etch residues remaining needs to be removed by stripping so that it does not interfere with any subsequent processing. The inventive stripping process for removing photoresist and/or post etch residues comprises generating an oxygen free plasma from a gas composition comprising a hydrogen bearing gas and a fluorine bearing gas by exposing the gas composition to an energy source capable of forming a plasma of the gas. The oxygen free plasma gas generates reactive species that selectively react with any photoresist and/or post etch residues remaining after the etching step to form a volatile compound. After stripping, the substrate is sometimes rinsed with deionized water to remove any remaining residues. The particular components of the oxygen free plasma gas are selected by their ability to form a gas and a plasma at plasma forming conditions. Preferably, the components are combined and added to the plasma asher as a gas. The oxygen free plasma gas reacts with carbon and other atoms in the photoresist compounds and post etch residues to form volatile compounds at conditions present in a plasma reaction chamber. Moreover, the oxygen free plasma reacts with those traditionally hard to remove post etch residues that contain silicon embedded in the residue.

CLAIMS:

3. A method for removing photoresist and/or post etch residues from a substrate comprising: a. placing at least one substrate having photoresist and/or post etch residues thereon into a wafer processing chamber; b. forming a reactive species by generating a plasma in the absence of oxygen wherein a gas for generating said plasma comprises a hydrogen bearing gas and a fluorine bearing gas; and c. selectively removing the photoresist and/or the etch residues including sidewall polymer depositions from an underlying layer in contact with the photoresist and/or post etch residues by exposing the substrate to said reactive species; d. said selectivity of etching by said plasma between the photoresist and/or post etch residues to the underlying layer is greater than about 10 to 1.

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